Proceedings of the 2007 IEEE
International Conference on Integration Technology
March 20 - 24, 2007, Shenzhen, China

Performance of Improved Three-Dimensional Turbo Product Code Decoder

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***Abstract*-Two-dimensional (2-D) turbo product code (TPC) has been investigated for almost ten years and commonly applied in recent years. In this paper, we propose improved schemes about three-dimensional (3-D) TPC decoder. Three different types of decoding methods are proposed, which do not simply decode by dividing the 3-D TPC into 2-D TPC, but exchange all the extrinsic information among three directions in order to achieve better performance. We bring up a parallel optimal decoder, which efficiently reduce the 3-D TPC decoding complexity. Simulation results show that the performance of the improved parallel 3-D TPC decoder is substantially improved. Various rates can be achieved by using different component codes or by applying shortening and puncturing techniques to meet diversified applications in modern communication systems. We also give the laws for code rate regulation and an example of 3-D TPC frame structure.**

Index Terms - Three-dimensional turbo product code, iterative decoding, serial decoder, parallel decoder

I. INTRODUCTION

Turbo code [1] is an excellent improvement in the field of the error-control coding but with a big limitation that it owns a high "error floor". That is, when the bit error rate is lower than 10e-6, it is very difficult to further improve the performance, especially for the short code length and code with the simple constructional component codes. The limitation obstructs the application of the Turbo codes in the some domain where reliability is overcritical in low Bit Error Rate such as magnetism channel.

Turbo product code (TPC), which was proposed in 1954 by Elias [2], is a powerful competition to Turbo code in the aforementioned problem. Due to the limited hardware resources, the code was restrictedly applied initially, and it was not until Pyndiah [3] improved the soft input soft output (SISO) decoding algorithm for TPCs based on the Chase algorithm that the study and application of the TPC have greatly progressed. Although the SISO is not optimal decoding algorithm for TPCs, it still reaches near optimum performance at low BER. In the past ten years, two-dimensional (2-D) TPC has been universally studied and it is even more widely applied than Turbo code for the powerful hardware supported by the AHA [4] company. Compared to Turbo code, the 2-D TPC owns many merits: it owns very low "error floor" deep into the level of 10e-7 or more; it can be encoded and decoded with very low complexity because it has no interleaver and adopts the suboptimal decoding algorithm; it performs so great that is nearly approach to the Shannon limit at high rate. From the point of view of capacity, the 2-D TPCs generally perform worse than Turbo codes in low SNR regions. It has been proved that the minimum Hamming distance of the TPC is given by the product of the minimum Hamming distance of component codes and does not depend on the block size. That means, the more component code is used, theoretically, the better performance it owns. Therefore, we believe that the 3-D TPCs deservedly have better performance.

In this paper we propose a scheme involving in the 3-D TPCs which can improve the TPC performance but with less additional complexity. In Section Ⅱ, we introduce the structure of 3-D TPCs. The basic and improved decoders of the 3-D TPCs are given in Section Ⅲ. In Section Ⅳ, simulation results are presented to prove the performance of 3-D TPC. In Section Ⅴ, the laws of regulating the code rate, which is important for the TPCs, are proposed with a typical example.

II. THE STRUCTURE OF 3-D TURBO PRODUCT CODE

Supposing C_i (i=1,2,3) be the coding scheme for the ith component code, the 3-D TPC $C = C_1 \times C_2 \times C_3$ in Fig. 1 can be obtained by:

(1) placing the $k_1 \times k_2 \times k_3$ information bits in a cube of k_1 length, k_2 width, and k_3 height;

(2) in the plane Z =0, coding the k_2 rows with C_1 along the X axes;

(3) in the plane Z =0, coding the n1 columns with C_2 along the Y axes;

(4) similarly, repeating (2)~(3) $k_3 - 1$ times, to accomplish the block coding in the plane Z=1,2,… $k_3 - 1$, which add to $k_3 - 1$ planes;

(5) coding the $n = n_1 \times n_2$ bits with C_3 along Z axes, which amounts to k3 times.

Parameters of the 3-D TPC are given by: $n = n_1 \times n_2 \times n_3$, $k = k_1 \times k_2 \times k_3$, $\delta = \delta_1 \times \delta_2 \times \delta_3$. The code rate is: $R = R_1 \times R_2 \times R_3$, where R_i is the code rate of C_i .

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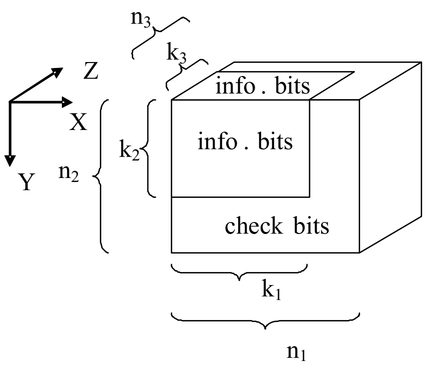

Fig. 1. The construction of 3-D TPC

The component codes Ci (i=1,2,3) may be Reed Solomon code, BCH code, or extended Hamming code [5]. Since 3-D TPC is encoded from three directions, we can reduce the check bits of each component code and choose component code with higher code rate. For example, the single parity code (SPC) can be adopted to achieve lowest decoding complexity [6].

TPC is efficient for burst error because the matrix (for 2-D) and cube (for 3-D) are natural interleavers. There are two ways to transmit the information bits: one is by length, width, and height of the cube, and the other is by diagonal or helix. The transmitting sequence is related to the ability to avoid burst error and different transmit method is corresponded to different decoding algorithm. Here, we adopt the former scheme.

III. THE ITERATIVE DECODING OF 3-D TURBO PRODUCT CODE

A. *Basic Serial Decoder*

The 2-D TPCs decoding algorithm is SISO algorithm based on modified Chase algorithm which has a very low complexity for double or even triple error correcting BCH codes. In this section we will introduce three type decoders for 3-D TPCs.

Firstly, let us consider the performance of the decoding of 3-D TPC based on the basic 3-D serial decoder. The information is transmitted over a Gaussian channel using BPSK signaling, on receiving cube [R] corresponding to a transmitted codeword [E]. The basic 3-D TPC serial decoder can be shown in Fig. 2. The first decoder performs the soft decoding along the X axes and the second (third) decoder does this along Y (Z) axes. By subtracting the soft input from the soft output we can obtain the extrinsic information [W(2)] ([W(3)]) where index 2(3) indicates that we are considering the information which was computed in the preceding decoder for the second (third) decoder.

The decoding process can be described as follows:

Step 1: initialization

$$[R(0)] = [R] \tag{1}$$

Step 2: iteration

$$[R(m)] = [R] + \alpha(m)[W(m)] \tag{2}$$

Denoted by the element in the cube:

$$r_j(m) = r_j + \alpha(m) w_j(m) \tag{3}$$

Where α and β (in the Fig. 2) are the same scaling factors in 2-D decoder. The parameters we set are: α=0.5, β=1.(Here, we mainly focus on the decoder's decoding process, and the optimal α and β can be found in [3].)

B. *Improved Serial Decoder*

The basic serial decoding scheme above is a simple extension of a 2-D decoder which gains some performance but not the best. The improved 3-D TPC serial decoder in Fig. 3 is an improved decoding scheme for the 3-D TPC with the better performance.

In the improved 3-D TPC serial decoder, we consider the X and Y axes as elementary belief decoders and the Z decoder as a high-level belief decoder. That means, the X and Y axes decoder is a 2-D TPC decoder and the Z axes decoder is an additional observer who synthesizes the extrinsic information from X and Y decoding precession and computes the exact result. The decoding process can be described as follows:

Step 1: initialization

$$[R_x(0)] = [R] \text{, } [R_y(0)] = [R] \text{, } [R_z(0)] = [R] \tag{4}$$

Step 2: iteration

$$[R_x(m)] = [R] + \alpha(m)[W_z(m)] \tag{5}$$

$$[R_y(m)] = [R] + \alpha(m)[W_x(m)] \tag{6}$$

$$[R_z(m)] = [R] + \alpha(m)[\lambda_1 W_x(m) + \lambda_2 W_y(m)] \tag{7}$$

Where λi (i=1, 2) is a standard factor to measure the weight of the extrinsic information of the X decoder and Y decoder. Best performance can be achieved by adjusting the value of λi .

C. *Improved Parallel Decoder*

The third type of the decoder present in Fig. 4 is an improved parallel decoder where all the element decoders do the decoding procession synchronously, depending on the soft output from the other two decoders as extrinsic information[7,8].

The decoding process can be rendered as follows:

Step 1: initialization

$$[R_x(0)] = [R];\ [R_y(0)] = [R];\ [R_z(0)] = [R] \tag{8}$$

Step 2: the 1st iteration

The three decoders do the decoding precession independently at one time.

Step 3: from the second iteration to the maximum number of iteration

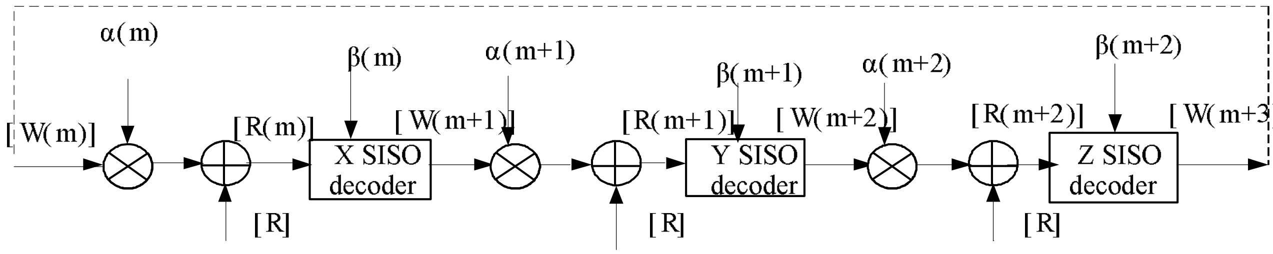

Fig. 2. The basic 3-D TPC serial decoder

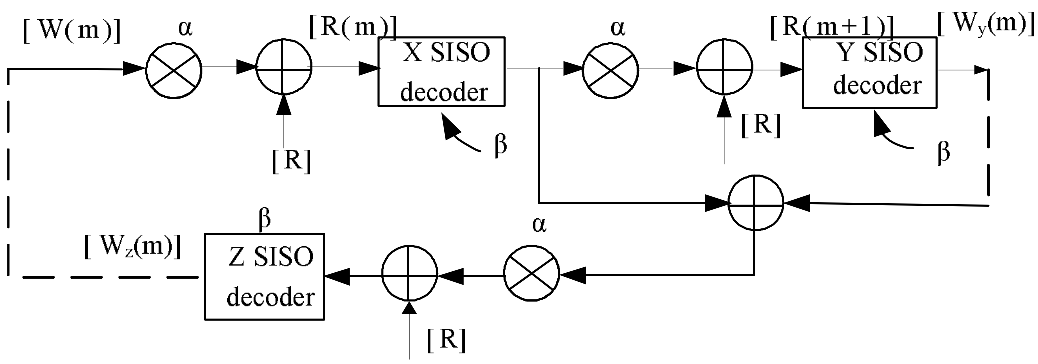

Fig. 3. The improved 3-D TPC serial decoder

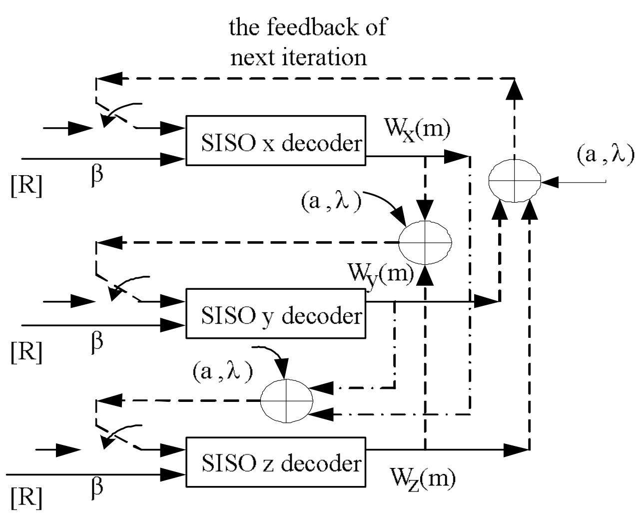

Fig.4. The improved 3-D TPC parallel decoder

$$[R_x(m)] = [R] + \alpha(m)[\lambda_{x1}W_y(m) + \lambda_{x2}W_z(m)] \quad (9)$$

$$[R_y(m)] = [R] + \alpha(m)[\lambda_{y1}W_z(m) + \lambda_{y2}W_x(m)] \quad (10)$$

$$[R_z(m)] = [R] + \alpha(m)[\lambda_{z1}W_z(m) + \lambda_{z2}W_x(m)] \quad (11)$$

Where λ_{ki} (i=1, 2; k=x, y, z) is a standard factor to measure the weight of the extrinsic information and best performance can be achieved by adjusting them.

The iterative decoding can be regarded as different observers evaluating the confidence of each bit from different perspectives and then exchange the information to achieve the most reliable results. To the improved parallel decoder, the observers (decoders) try their best to exchange the extrinsic information, and naturally gain the best performance. Since the decoding in the three decoders can be done at the same time, it doesn't add much complexity and saves the decoding time.

IV. SIMULATION RESULTS

Fig. 5 shows the influence of the maximum number of iteration to the decoders. The component code we choose is (15, 11, 3) BCH code and the decoding scheme is a basic 3-D TPC serial decoder. It is clear that the FER performance is also improved by increasing the maximum number of iteration.

The performance comparison of 3-D TPC decoders based on the basic serial decoder, the improved serial decoder and the improved parallel decoder is shown in Fig. 6. The component code we choose is still a (15, 11, 3) BCH code and the number of iteration is 16. As we all know, for 2-D TPCs,

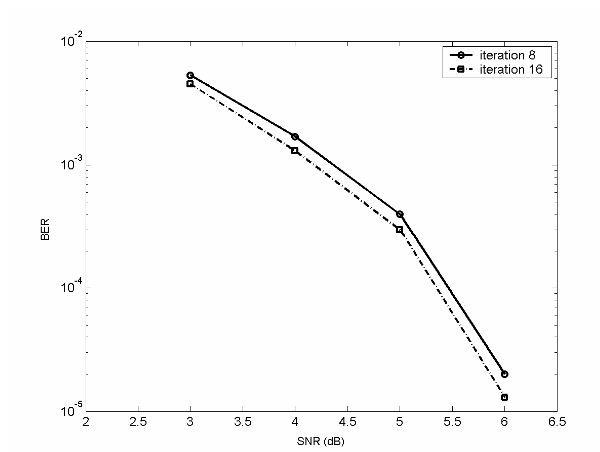

Fig.5. The FER performance of a basic 3-D TPC serial decoder with various number sof iteration

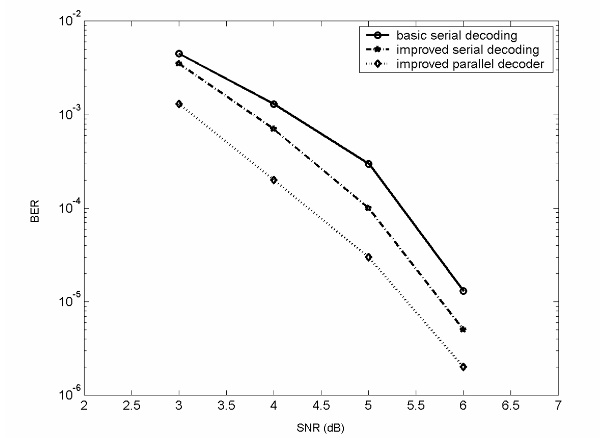

Fig.6. The performance comparison of the 3-D TPC decoders

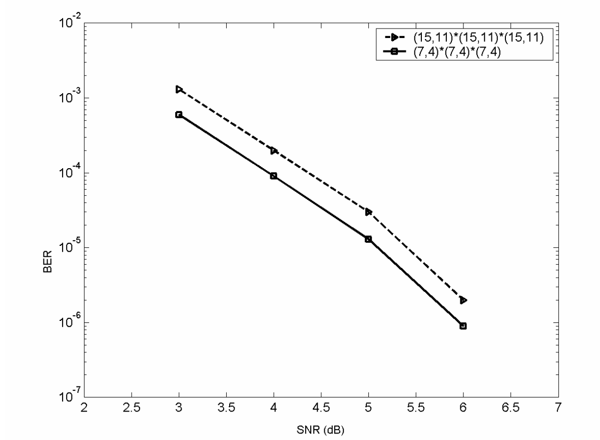

Fig.7. The performance of a improved 3-D TPC parallel decoder with various code lengths

there is so much difference between the serial and parallel decoders. But for 3-D TPC, the parallel decoder has the best performance to the others. Since it also saves the decoding time, we consider it as an optimal scheme.

Fig. 7 describes the 3-D TPC with various code lengths. The code with low rate owns better performance. (The decoding scheme we used is an improved parallel decoder and the number of iteration is set 16.)

V. THE CODE RATE REGULATION

TPC can be designed for various rates [5] and when the channel environment is worse, lower rate can be adopted to reduce BER without bandwidth expense, and all the codes with different rates can be decoded on the same decoder.

We propose some rules for the TPC's code rate regulation：

1. If possible, we puncture more check bits rather than information bits.
2. If the component codes C^i are different, we puncture more bits of the component code C^i whose code rate is higher.
3. It is better to remove the outer rows or columns in the cube.
4. It is better to remove the first information bits in a row (column) during fine regulation.

In Fig. 8 we give an illustration of the 3-D TPC 's code rate regulation for the frame (2544, 1096). The original code is a (32, 26) × (32, 26) × (4, 3) code. Firstly, we cut off 6 plane bits from X=0 to X=5 along X axes, then 7 planes bits from Y=0 to Y=6 along Y axes to get a (26, 20) × (25, 19) × (4, 3) code. Now the information bit sum is 1140, all the bits are 2600. It still needs to be regulated. 14 information bits are needed puncturing: at Z=0 plane, removing 2 rows bits along X axes (20 bits each row), then another 4 bits in the next row, remaining 1140-44=1096 (information bit).

In the foregoing procedure, with 12 check bits (6 each row) bit off, the total bit remaining is 2600-44-12=2544. The code rate is k/n=1096/2544=0.43. Apparently according to the laws aforementioned, it is easy to regulate any 3-D TPCs to proper code rates.

VI. CONCLUSIONS

In this paper, we proposed performance of improved 3-D TPC decoder, where 3-D TPC decoder inherits all the 2-D TPC's advantages, and has a better performance in low SNR environment. Simulation results show that the improved 3-D TPC parallel decoder can not only perform much more quickly and exactly than the other 3-D TPC decoders, but also solve the decoding complexity of the 3-D TPC. With all these predominance above as well as the various rates available for diversified applications, the 3-D TPC has been one of most promising schemes in the future mobile communication systems.

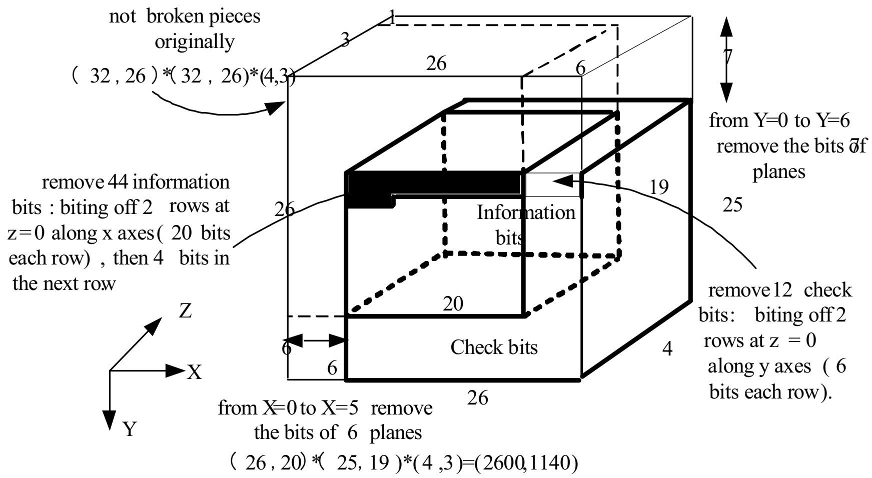

Fig.8 An example of 3-D TPC's code rate regulation

ACKNOWLEDGMENT

The work was supported by the National Natural Science Foundation of China (No. 60496315) and a grant from the Research Grants Council of The Hong Kong Special Administrative Region.

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